memory location of an operand on which the instruction operates. These two addresses are **different** memory locations. The operand value is stored at a **different** memory location from the instruction. Thus, the operand address is different from the instruction address (emphasis in original)."

The Office Action maintains that an operand address and an instruction address are the same address. *See* Office Action, page 4, lines 20-22. Specifically, at page 2, the Office Action asserts that an "operand address" is mere data/information in a trace buffer. This is only the binary bits stored in the trace buffer called traced information." The Office Action thus contends that the only difference between the claimed invention and Circello is printed matter (i.e., the binary bits in the trace buffer). Applicants respectfully disagree.

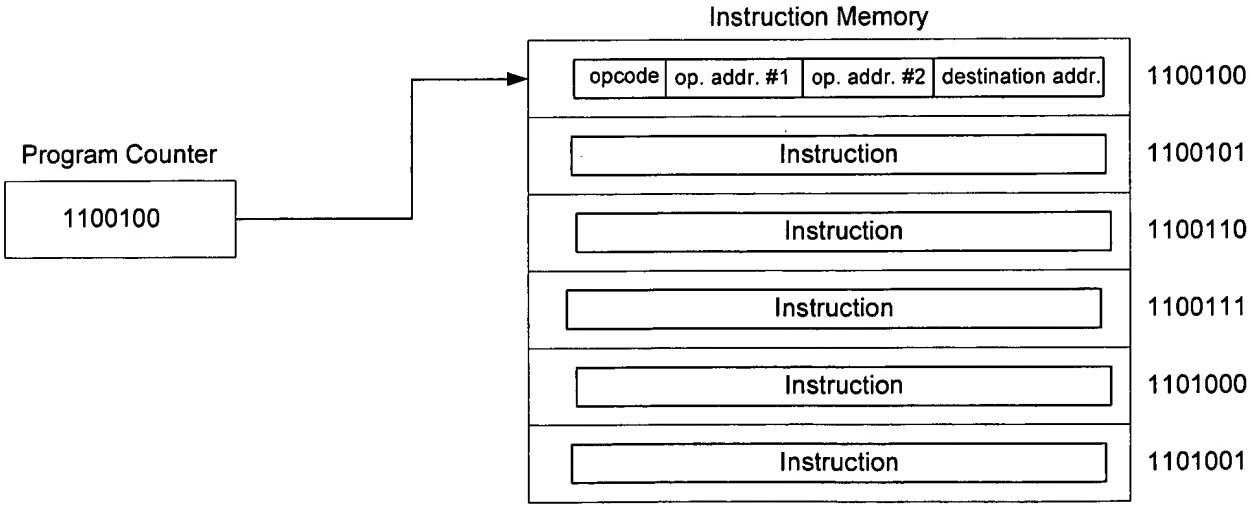
The Office Action cites MPEP §2112.01 which states that, "[w]here the only difference between a prior art product and a claimed product is printed matter that is not functionally related to the product, the content of the printed matter will not distinguish the claimed product from the prior art." Applicants respectfully disagree that an operand address is printed matter. Rather, the operand address is a series of electrical signals. Additionally, even if one were to consider the operand address to be printed matter, the operand address is functionally related to the claimed system as the operand address is transmitted over the communication link. Thus, MPEP §2112.01 is not applicable to the claims of the present invention.

The Office Action further asserts that "the recitation 'operand address' in the Claims is only an intended use and operand address does no structure different in compared to whatever data stored in the trace buffer of Circello." *See* Office Action, page 3. Applicants respectfully disagree that the recitation of the term "operand address" is an intended use. Using claim 1 as an example, the term "operand address" is used in a functional limitation that defines how the processor operates. Specifically, claim 1 recites, "a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address." Thus, the term "operand address" is a functional limitation to indicate that the processor transmits an operand address to the debug

circuit via the communication link. This limitation does not recite an intended use, but is rather a functional limitation that defines how the processor operates.

Further, at page 4, the Office Action asserts that there is no difference between an operand address and an instruction address. The Office Action contends that, "'operand address' or 'instruction address' is only the binary data value obtained from the program counter. In Circello's column 22, within the table in line 27-35, it shows very clearly the meaning of 'instruction address' (right). It is a value of the program counter. Each value points to a location of an 'instruction.' Each instruction may include an operator (such as Add, Mul, or Mov) and its operands. The Applicants' argument that 'These two addresses are different memory locations' is incorrect (emphasis in original)."

Applicants respectfully maintain that the instruction address that is sent from the processing core 9 to the debug module 10 in Circello **is not an operand address**. To aid in clarifying what information is transmitted from the processor core 9 to the debug module 10 in Circello, Applicants provide an example of the way that the system of Circello is understood to operate using the diagram below.



The diagram above shows a program counter and an instruction memory that stores a plurality of instructions. The value of the program counter is an instruction address that indicates the address in memory of the next instruction to be fetched. In the example above, the value of

the program counter is "1100100." Thus, the next instruction to be fetched is the instruction stored at the memory address "1100100." That is, the value "1100100" is an instruction address. As shown in the diagram above, the instruction stored at instruction address "1100100" includes an opcode, which defines what operation is to be performed, two operand addresses, which indicate the memory locations of the operands on which the operation is to be performed, and a destination address, which indicates the memory location of the result
Thus, the instruction stored at memory address "1100100" may be an add instruction as shown in the diagram below.

opcode	op. addr. #1	op. addr. #2	destination addr.
ADD	110010	111010	1000010

That is, the opcode of the instruction indicates that an add operation is to be performed. The location of the operands to be added in the add operation is also indicated in the instruction. That is, the first operand is stored at memory address "110010" and the second operand is stored at memory address "111010." The instruction also indicates the address of the memory location where the result of the add operation is to be stored (i.e., memory address "1000010").

Circello discloses that instruction addresses are provided from the processor core 9 to the debug module 10, **but does not disclose or suggest that an operand address is provided from the processor core 9 to the debug module 10**. Thus, from the perspective of an external user who is debugging a program, the user could, for example, step through execution of the program and, when the user reaches the add instruction shown above, the user would be able to see the address in memory at which the add instruction is stored (i.e., the instruction address), but would not be able to see the addresses in memory at which the operands are stored.

Thus, referring to the example provided by the diagrams above, an external user who is debugging a program would be able to see the instruction address of the ADD instruction (i.e., "1100100"), but would be unable to see the operand addresses (i.e, "110010" and "111010").

None of the signals that Circello discloses as being transmitted from the processor core 9 to the debug module 10 include an operand address. Figure 1 of Circello shows that a Bus Grant

signal may be transmitted from processing core 9 to debug module 10 which is used by CPU 2 of processing core 9 to indicate to debug module 10 that it has been granted use of K-Bus 25 (Col. 29, lines 41-55). Further, a CPU Processor Status (CPST) signal may be transmitted from processing core 9 to debug module 10 that indicates the type of operation currently being executed by data processor 3 (Col. 18, lines 47-53). For example, the CPST signal may indicate when execution of an instruction begins, when execution of an instruction should continue, when data processor 3 enters into a selected mode of operation, when a preselected branch instruction is executed, and when operation of data processor 3 is halted (Col. 18, lines 53-60).

Additionally, several signals may be transmitted from processing core 9 to debug module 10 over K-Bus 25 (Col. 4, lines 62-63). The signals transmitted over K-Bus 25 are KADDR, KDATA, and KCONTROL (Col. 4, lines 63-65). The KADDR signal is used to send instruction addresses accessed during normal operation of data processor 3 to debug module 10 and the KDATA signal is used to send operand values to debug module 10 (col. 18, lines 25-31). Circello does not explicitly disclose how the KCONTROL signal is used. None of these signals includes operand address information.

As should be clear from the discussion above, Circello does not disclose or suggest transmitting an operand address from the processor core 9 to the debug module 10. Accordingly, it is respectfully requested that the rejection of claims 1-64 under 35 U.S.C. §102 be withdrawn.

CONCLUSION

In view of the foregoing remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

David Alan Edwards, et al., Applicants

By: _____

James H. Morris, Reg. No.: 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Telephone: (617) 720-3500

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